VLSI Architecture for Hierarchical Temporal Memory

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Abstract: A large number of real world applications, such as image recognition and understanding, can still not be performed easily by conventional algorithms in comparison with the human brain. Implementing applications that require such intelligence, might therefore require a different approach, for which Hierarhical Temporal Memory (HTM) seems a promising framework. Currently HTM exists as a software model. However, this software implementation has its performance limitations and a distinct learning and operating mode. This paper proposes a possible architecture for VLSI implementation that also allows learning during normal operation.